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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,344	04/15/2004	Hiroyuki Kanda	2004_ 0586A	6329
513 7590 04/30/2008 WENDEROTH, LIND & PONACK, L.L.P. 2033 K STREET N. W. SUITE 800 WASHINGTON, DC 20006-1021				
EXAMINER				
LEADER, WILLIAM T				
ART UNIT		PAPER NUMBER		
1795				
MAIL DATE		DELIVERY MODE		
04/30/2008		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/824,344

**Applicant(s)**

KANDA ET AL.

**Examiner**

WILLIAM T. LEADER

**Art Unit**

1795

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 February 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-946)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 6, 2008, has been entered.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin et al (US 6,432,821) in view of Ueno (US 6,245,676).

5. The Dubin et al patent (hereinafter Dubin) is directed to an electroplating process for filling damascene structures such as trenches and vias on a semiconductor wafer. The structures include a range of sizes from small to large. See the abstract. This corresponds to the first step recited in instant claim 1. The wafer is immersed in a copper electroplating solution (column 5, lines 4-7). The solution contains an accelerator additive which may be an organic compound such as sulfopropyl disulfide or mercaptopropanesulfonic acid (column 3, lines 56-60). Forward electric current is supplied to electroplate copper and perform a superfill operation (bottom-up filling) to fill the smallest damascene features. These features have, for example, openings less than 0.3  $\mu\text{m}$  (column 5, lines 16-20). This corresponds to the second step recited in claim 1. After the plating step, a reverse electric current is applied to perform a reverse plating operation which removes adsorbed plating additives from the wafer (column 5, lines 20-23). This corresponds to the third step recited in claim 1. A second plating step is performed to fill

damascene features having, for example, openings about 0.3 to 0.6  $\mu\text{m}$  (column 5, lines 24-27). This corresponds to the last step recited in claim 1.

6. Instant claim 1 differs from Dubin by reciting that the reverse electric field is applied for the specific time range of 1 second to 4 seconds. In the process of Dubin, the electric power supplied to the wafer being plated is illustrated in figure 7. The forward current steps may be applied for a time between 2 and 60 seconds (column 5, lines 41-43). With this time frame, figure 7 suggests that the reverse current is applied for a time in the range of a few seconds. However, Dubin is silent as to an exact numerical value.

7. The Ueno patent is directed to electroplating copper into trenches to form interconnects on a silicon wafer. See the abstract. As shown in Figure 4, Ueno applied reverse polarity current to remove additive molecules. See also column 9, lines 42-47 which teach applying a back bias current to remove adsorbed additive molecules. The duration of the reverse polarity current pulse  $t_2$  is within about 10 seconds (column 10, lines 13-15). This range of less than about 10 seconds encompasses applicant's claimed range of 1-4 seconds. The prior art of record is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious at the time the invention was made to have applied reverse current in the process of Dubin for the purpose of removing accelerator molecules for a time period of 1-4 seconds because Ueno teaches that reverse current applied for this time is

effective to remove additive molecules. Choice of a range, such as 1 to 4 seconds, within the range disclosed by Uneo would have been obvious to one of ordinary skill in the art since Uneo suggests that all times within the range are effective.

8. With respect to claim 2, Dubin discloses that in a damascene process a seed layer is formed before copper is plated (column 2, lines 12-14). With respect to claim 4, as noted above, the small features of Dubin have a width of less than 0.3  $\mu\text{m}$ . This includes the range of less than 0.2  $\mu\text{m}$  recited in claim 4. With respect to claims 5 and 6, the abstract of Dubin refers to small and large features (plural) which clearly suggests a plurality of features. With respect to claims 7-9, Figure 7 of Dubin illustrates the use of a higher current density to fill the larger openings than the current density used to fill the smaller openings. The current densities may be in the range of 10-30  $\text{mA}/\text{cm}^2$  (1-3  $\text{A}/\text{dm}^2$ ). See column 5, lines 41-43. The lower end of the range used for filling the smallest openings is within the range of 0.1-1.5  $\text{A}/\text{dm}^2$  recited in claim 9, while the upper end of the range used for filling larger openings is within applicant's range of 2-7  $\text{A}/\text{dm}^2$ . The current densities used by Dubin would provide conditions for relatively high bottom-up capability in the first plating step and relatively high leveling capability in the second plating step as recited in instant claim 3 in the same way as applicant's increasing current density.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM T. LEADER whose telephone number

is (571) 272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Susy Tsang-Foster can be reached on 571-272-1293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Harry D Wilkins, III/  
Primary Examiner, A.U. 1795

/William Leader/  
April 25, 2008